

Multi-Dimensional Analysis of Software Power Consumptions in Multi-Core Architectures

Maxime Colmant — PhD Defense — 24th November, 2016

Jury:

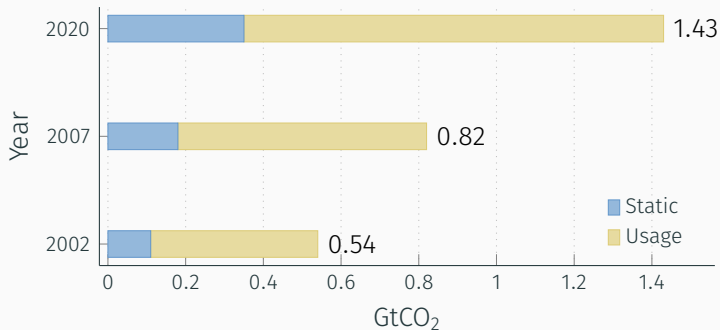
Mr.	Olivier	BARAIS	UNIVERSITY RENNES 1	Reporter
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Mr.	Giuseppe	LIPARI	UNIVERSITY LILLE 1	Examiner
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Mr.	Alain	ANGLADE	ADEME	Guest

TABLE OF CONTENTS

1. Introduction
2. Contributions
3. Conclusion & Perspectives

INTRODUCTION

THE GLOBAL ICT¹ FOOTPRINT²



¹Information and Communications Technology

²The Climate Group. *SMART 2020: Enabling the low carbon economy in the information age*. 2008.

MULTI-CORE CPU ARCHITECTURES ARE EVERYWHERE!



Smartphone



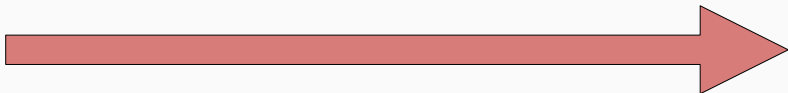
Laptop



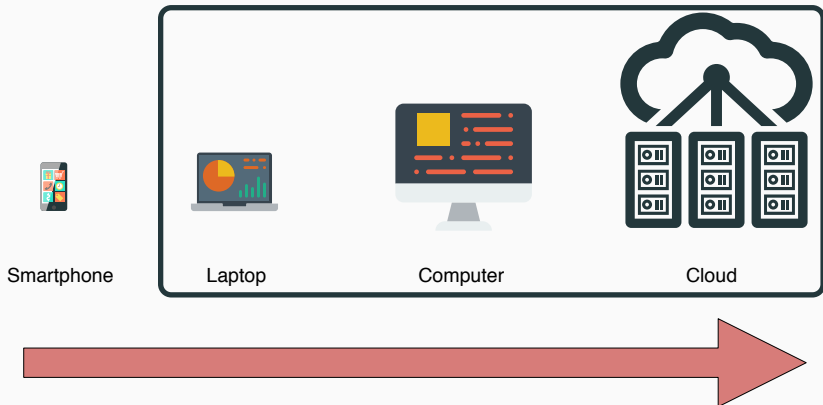
Computer



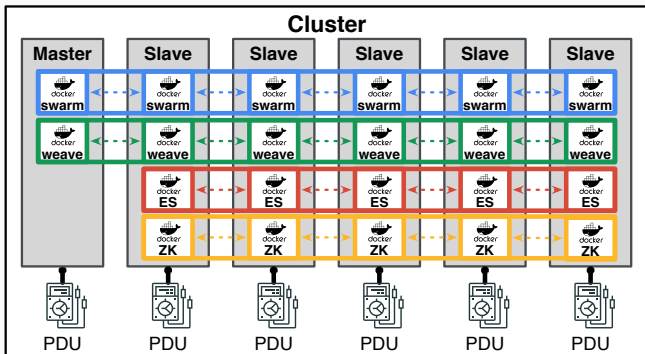
Cloud



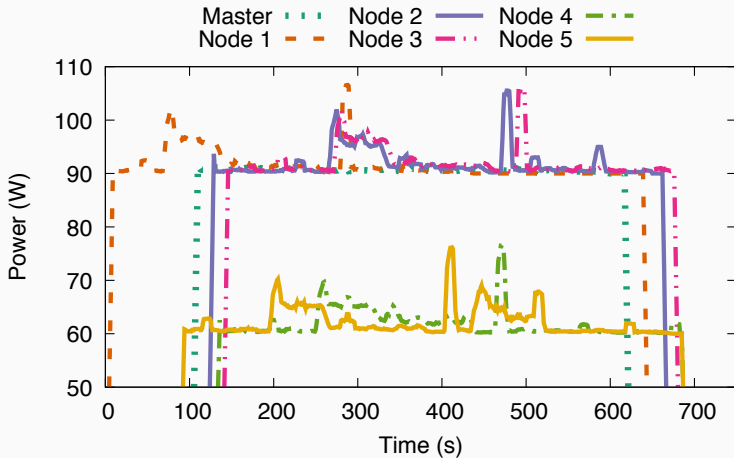
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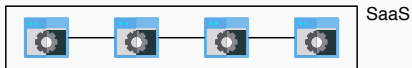
CASE STUDY



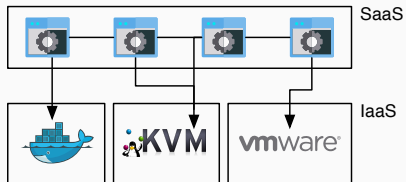
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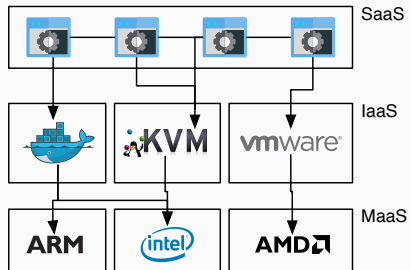
WHAT IS A MULTI-CORE SOFTWARE SYSTEM?



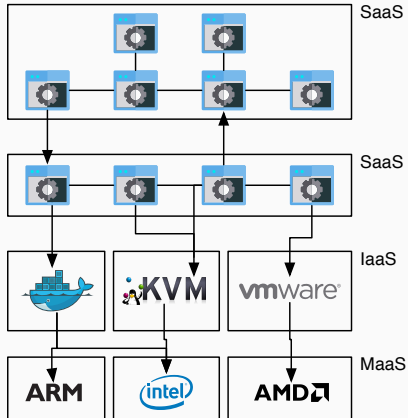
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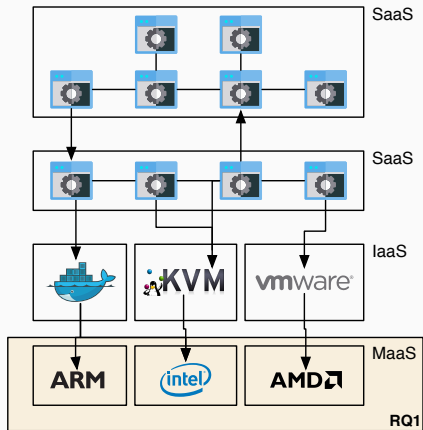


WHAT IS A MULTI-CORE SOFTWARE SYSTEM?



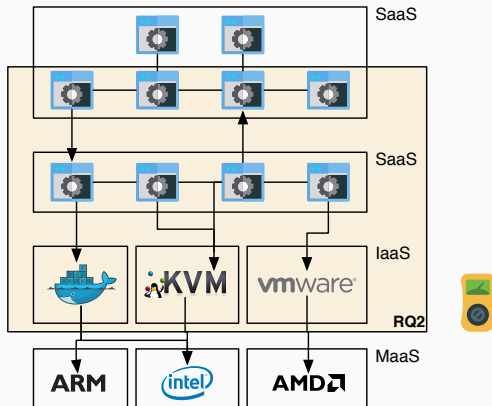
RESEARCH QUESTIONS

RQ1: Can we model the software power consumption regardless of the underlying architecture?



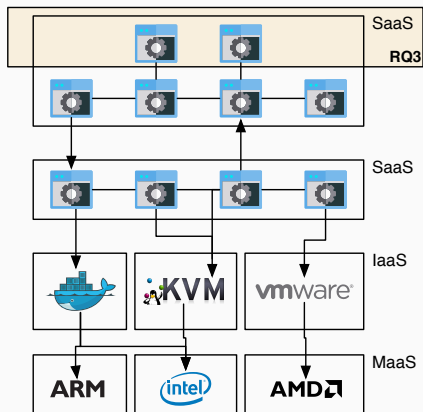
RESEARCH QUESTIONS

RQ2: Can we propose a uniform view of the service power consumption?



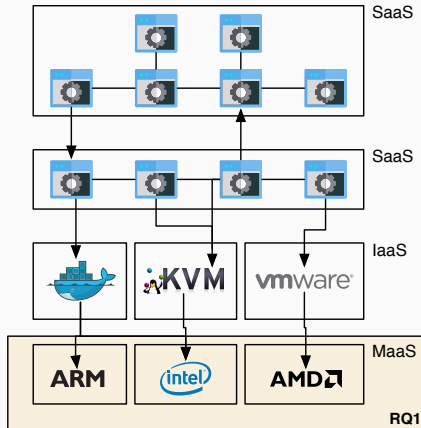
RESEARCH QUESTIONS

RQ3: Can we analyze the power consumption of the artifacts which compose a software?

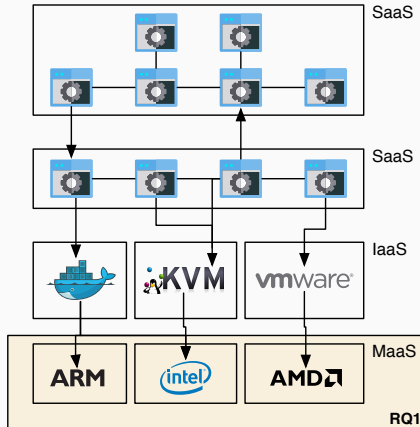


CONTRIBUTIONS

RQ1: Can we model the software power consumption regardless of the underlying architecture?



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Learning CPU Power Models

WHAT IS A POWER MODEL?

- Math. function (metrics) \Rightarrow Power

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- CPU metrics

From HW sensors (motherboard, power meters)

From Hardware Performance Counters (HPCs)

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From HW sensors (motherboard, power meters)

From Hardware Performance Counters (HPCs)

- [Nou14]³: $P_{cpu}^{app} = 0.7 * TDP * CPU_{stats}$

³A. Nouredine. "Towards a Better Understanding of the Energy Consumption of Software Systems". PhD thesis. Université des Sciences et Technologie de Lille - Lille I, 2014.

EXISTING CPU POWER MODELS

Ref.	Processor(s)	Feature(s)	Regression(s)	Benchmarks
[Ber+10]	Core 2 Duo	14 PCs regrouped by component	multiple linear by component	<i>sampl.</i> : μ -benchs <i>eval.</i> : SPEC CPU 06
[Col+15]	Xeon W3520 & i3 2120	non-halted cycles reference cycles	polynomial	<i>sampl.</i> : stress <i>eval.</i> : PARSEC, SPECjbb
[CM05]	XScale PXA255	5 PCs	multiple linear	<i>eval.</i> : SPEC CPU 00, Java CDC/CLDC
[Dol+15]	Xeon E3-1275	3 PCs HW sensors	linear	<i>sampl.</i> : linpack, stream, iperf, IOR <i>eval.</i> : Quantum Espresso
[ERK06]	Turion, Itanium 2	HW sensors	multiple linear	<i>sampl.</i> : Gamut <i>eval.</i> : SPECS, Matrix, Stream
[IM03]	Pentium 4	15 PCs	multiple linear	<i>eval.</i> : μ -benchs, AbiWord, Mozilla, Gnumeric
[RRK08]	Core 2 Duo & Xeon, Itanium 2, Turion	HW sensors PCs	multiple linear	<i>sampl.</i> : calibration suite <i>eval.</i> : SPECS, stream, Nsost
[Yan+14]	Xeon E5620 & E7530	7 components 91 preselected	support vector	<i>sampl.</i> : NPB, IOzone, CacheBench <i>eval.</i> : SPEC CPU 06, IOzone
[Zha+14]	Sandy Bridge	non-halted cycles	linear	<i>eval.</i> : Google, SPEC CPU 06
???	ARM	???	???	???

Only for Intel or AMD architectures

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HW sensors: coarse-grained CPU metrics

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HPCs: fine-grained CPU metrics

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Power models are mostly linear

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Non free or private workloads

1. Portability

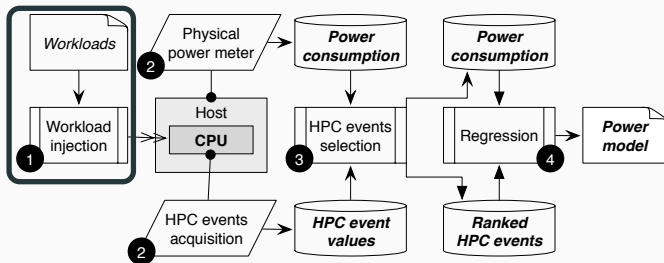
1. Portability
2. Accuracy

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3. Reproducibility

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Towards an automatic approach for learning CPU power models

OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

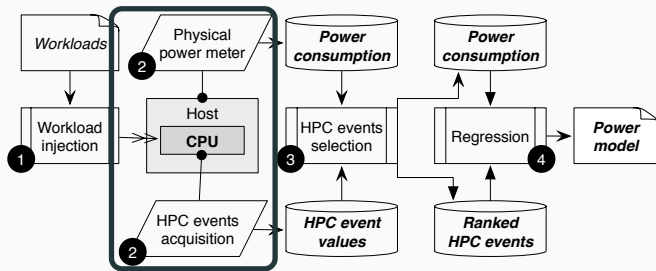


1 Input workload injection

- Configurable
- PARSEC (open-source, multi-threaded)⁴
- Run several applications (x264, vips, etc.)

⁴C. Bienia et al. "PARSEC 2.0: A New Benchmark Suite for Chip-Multiprocessors". In: *Proceedings of the 5th Annual Workshop on Modeling, Benchmarking and Simulation*. 2009.

OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

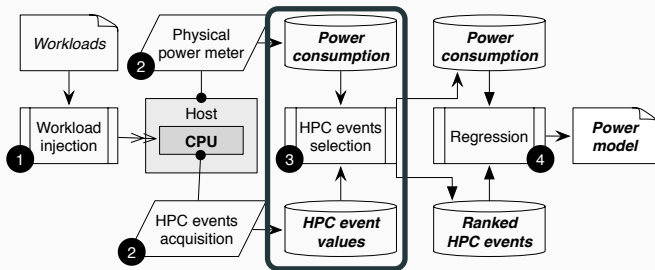


2 Acquisition of raw input metrics

- Automatically explore the high number of the available HPCs (Xeon W3520: 514 HPCs)
- Take care of HPC multiplexing⁵

⁵Intel. *Intel 64 and IA-32 Architectures Software Developer's Manual*. 2015.

OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

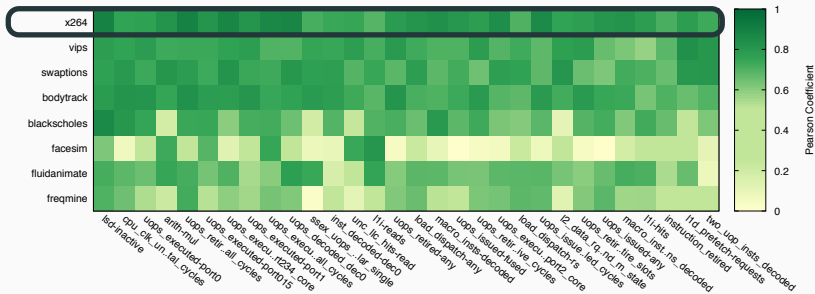


3 Selection of relevant HPCs

- Pearson coefficient (HPC \Leftrightarrow Power)
- 1st phase: quickly filtering out uncorrelated HPCs (< 0.5)
(Xeon W3250: 253 left out)
- 2nd phase: full sampling for the remaining HPCs

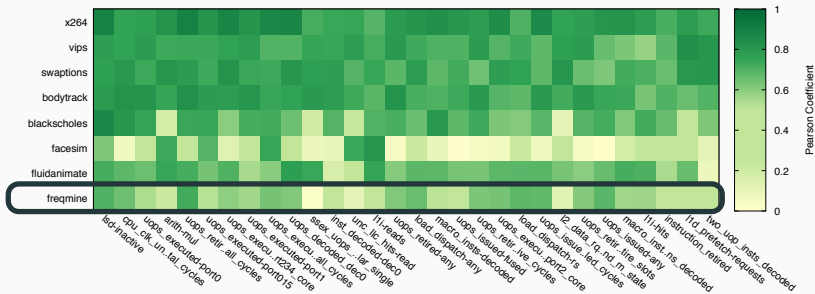
OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

Pearson coefficients of the Top-30 correlated events for the PARSEC benchmarks on a Xeon W3520.



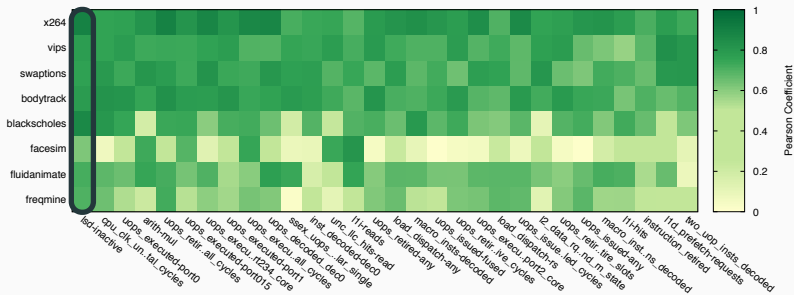
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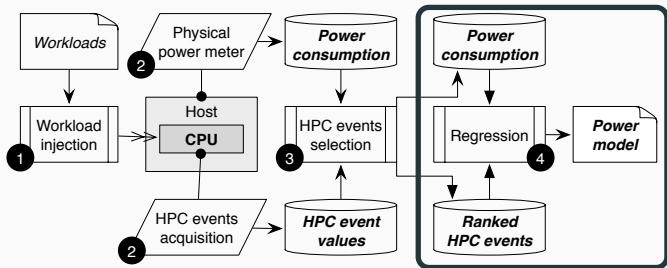


OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

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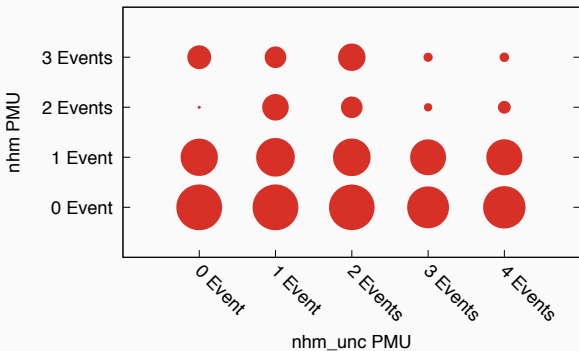
4 Power model inference

- Minimize the number of HPCs
- Robust ridge regression (SotA?)

OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

Average error per combination of HPCs for `freqmine`, `fluidanimate`, `facesim` on a Xeon W3520.

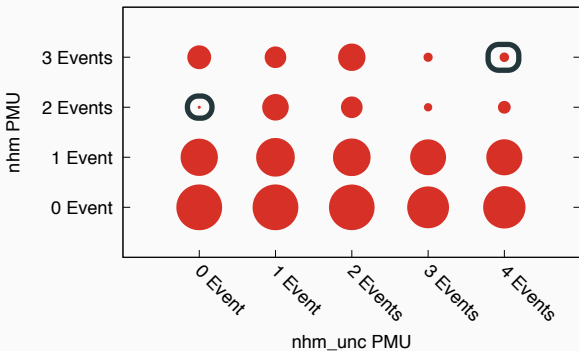
$$P_{idle} = 92 W ; P_{CPU} = \frac{1.40 \cdot \text{HPC (l1i:reads)}}{10^8} + \frac{7.29 \cdot \text{HPC (lsd:inactive)}}{10^9}$$



OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

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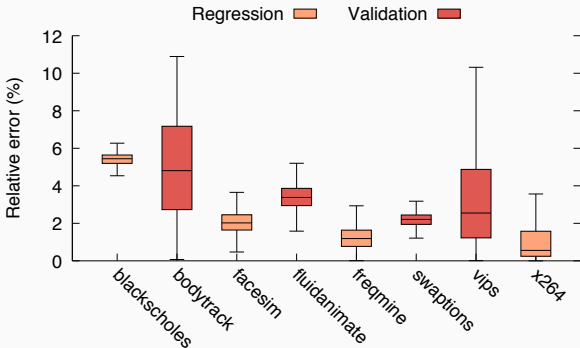
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OUR APPROACH: OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS

Relative errors for the PARSEC suite on the Cortex A15.

$$P_{idle} = 3.5 W ; P_{CPU} = \frac{1.18 \cdot \text{cpu_cycles}}{10^9} + \frac{1.26 \cdot \text{inst_spec_exec_integer_inst}}{10^{10}} + \frac{1.84 \cdot \text{bus_cycles}}{10^{11}}$$



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Beyond SotA: 4 CPUs (2×Intel, 1 AMD, 1 ARM)

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Built on open-source workloads

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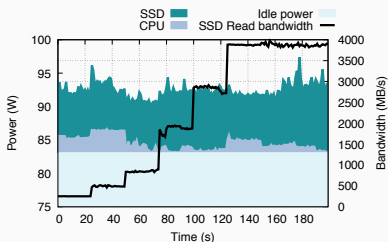
- **Extensibility**

Can we extend our learning approach to SSD power models?

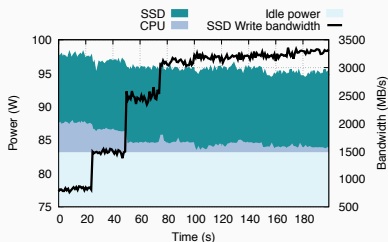
MOTIVATION

Comparison of power consumptions between CPU and SSD by varying the throughput with the `fiio` tool.

(a) SSD read operations.

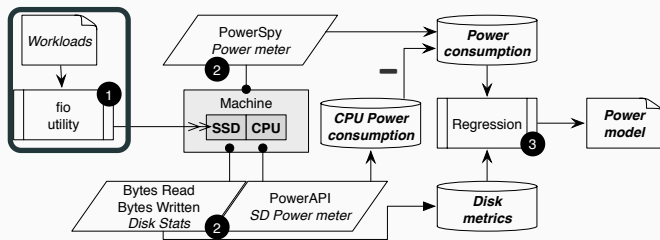


(b) SSD write operations.



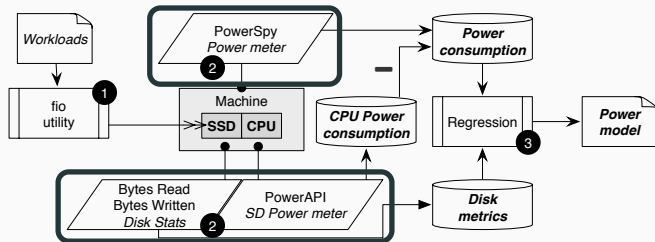
OUR APPROACH:

OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS (2)



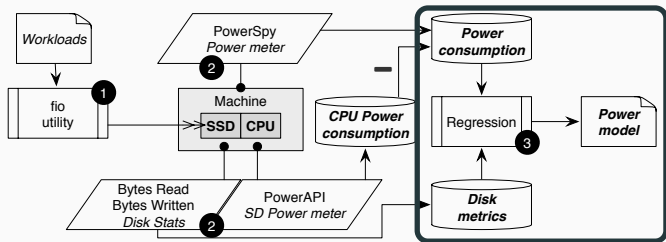
OUR APPROACH:

OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS (2)



OUR APPROACH:

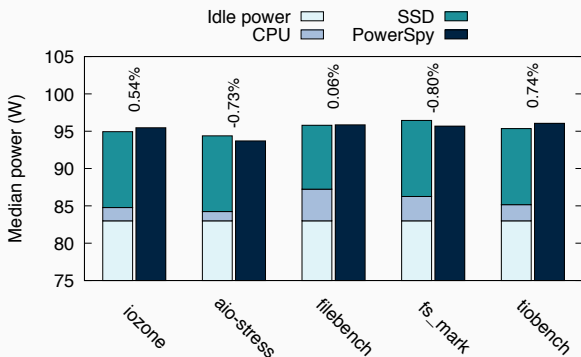
OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS (2)



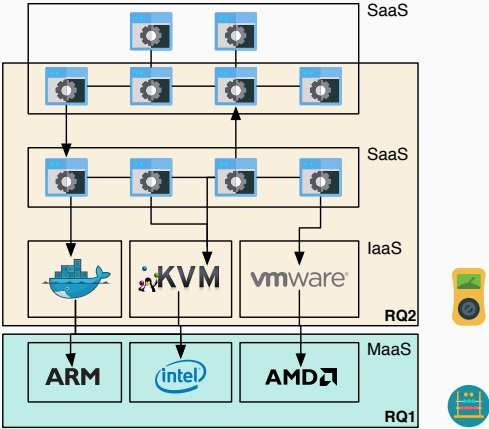
OUR APPROACH:

OPEN-TESTBED TO AUTOMATICALLY LEARN POWER MODELS (2)

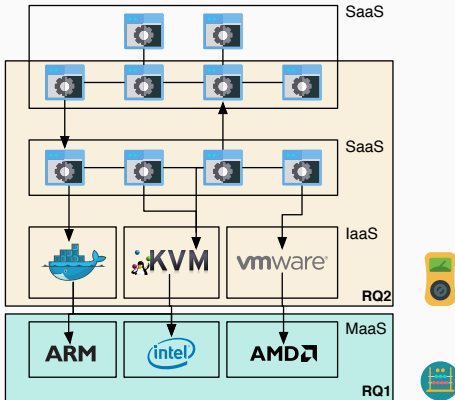
Power consumption of the host for 5 workloads on a Xeon E5-2630.



RQ2: Can we propose a uniform view of the service power consumption?



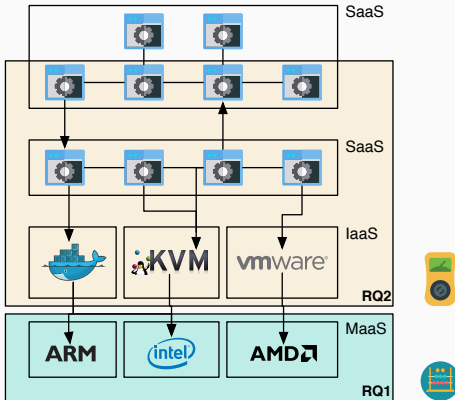
RQ2: Can we propose a uniform view of the service power consumption?



Challenges

1. Native
2. Virtualized
3. Distributed

RQ2: Can we propose a uniform view of the service power consumption?



Challenges

1. **Native**
2. Virtualized
3. Distributed



- Code freely available on GITHUB: <http://powerapi.org>
 - Scala / Akka
 - LoC: 8.7k
 - Docker
 - AGPLv3

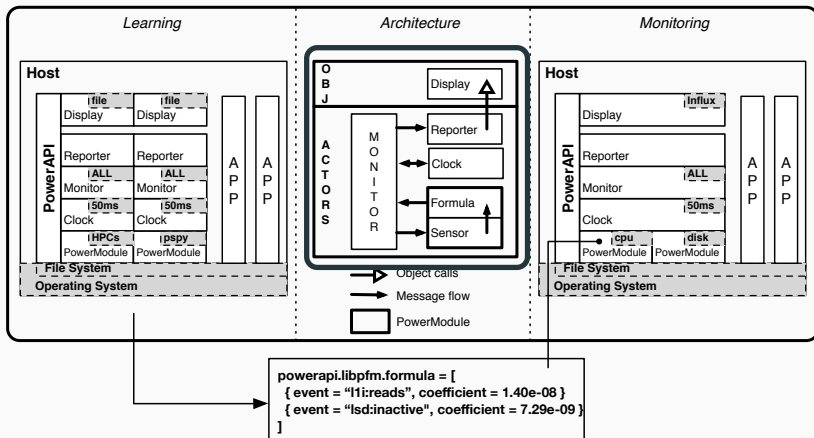
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- 2nd major iteration⁶
 - Full support of multi-core CPU architectures (HT, DVFS, TB)
 - Learning techniques
 - Better support of Akka

⁶A. Nouredine. “Towards a Better Understanding of the Energy Consumption of Software Systems”. PhD thesis. Université des Sciences et Technologie de Lille - Lille I, 2014.

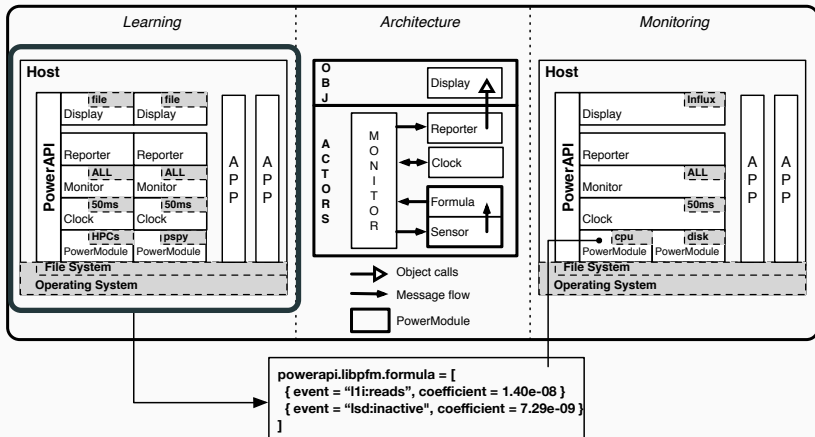
POWERAPI: A TOOLKIT FOR BUILDING SD POWER METERS

POWERAPI's architecture & deployment.



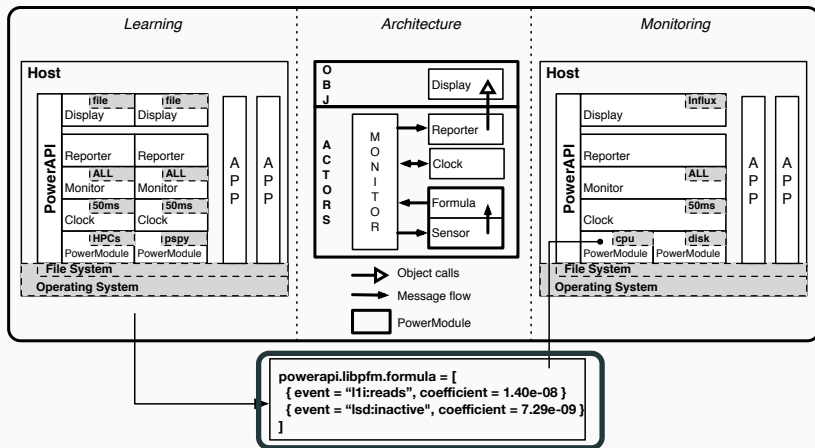
POWERAPI: A TOOLKIT FOR BUILDING SD POWER METERS

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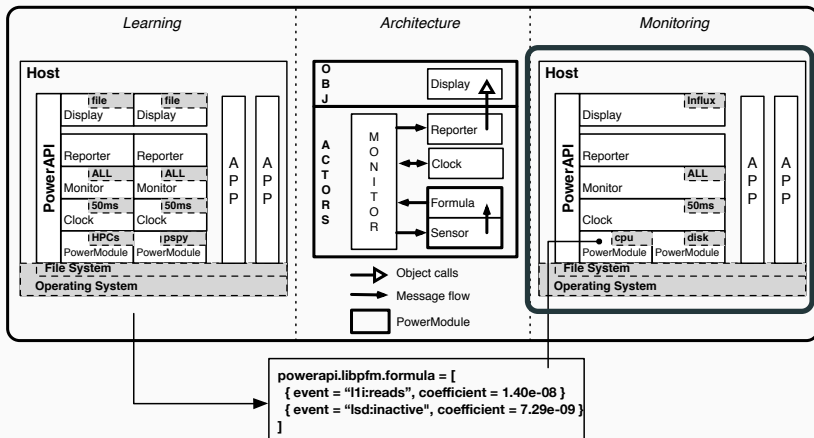
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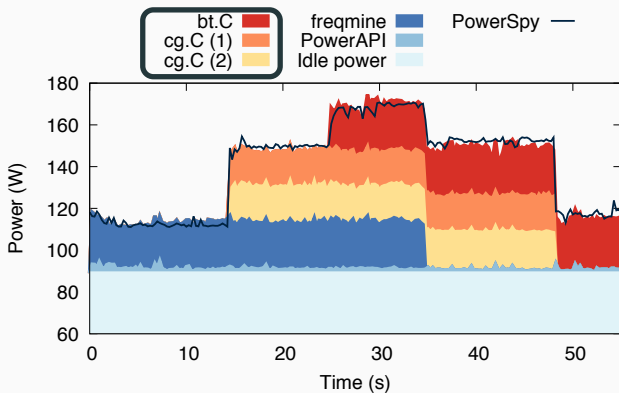


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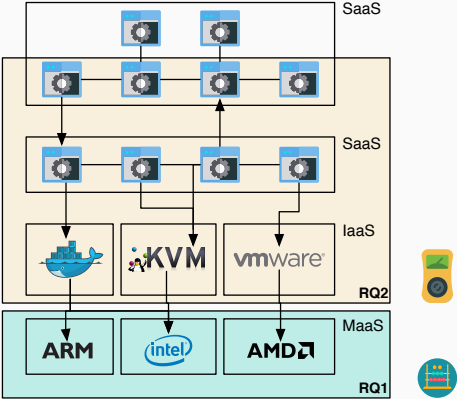


SD POWER METER FOR MONITORING CONCURRENT APPS



- On the Intel Xeon W3520
 - Monitoring freq.: 4Hz
 - Avg. error: 2%
 - Low overhead: 2 W

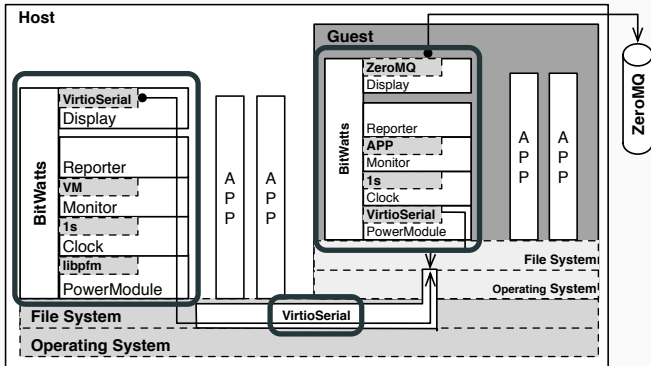
RQ2: Can we propose a uniform view of the service power consumption?



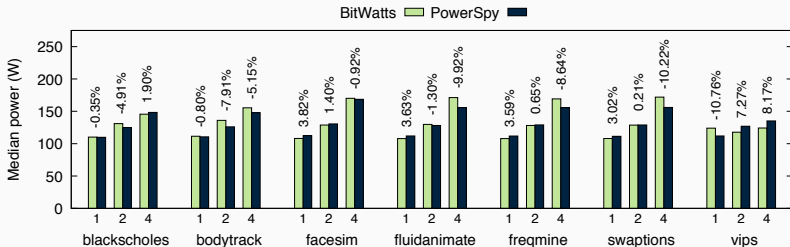
Challenges

- 1. Native
- 2. Virtualized
- 3. Distributed

BITWATTS ARCHITECTURE



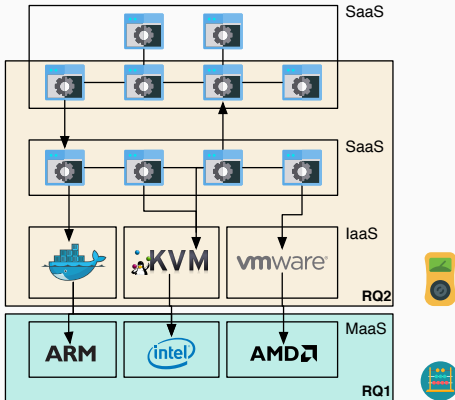
Scaling PARSEC on multiple VMs on a Xeon W3520.



- Errors: from 1% (fluidanimate) up to 10% (swaptions)
- Beyond SotA [Ber+12]:⁷ VM as a White-Box (+ multi-tenant)

⁷R. Bertran et al. "Energy Accounting for Shared Virtualized Environments Under DVFS Using PMC-based Power Models". In: *Future Generation Computer Systems* (2012).

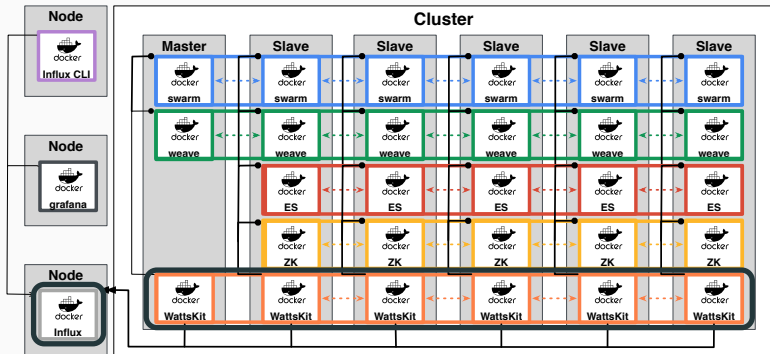
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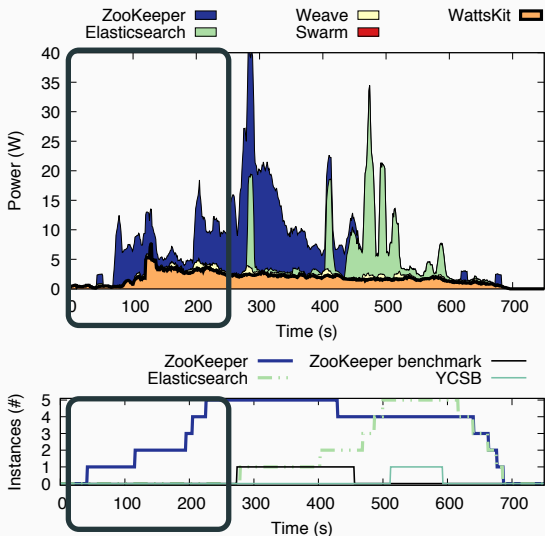
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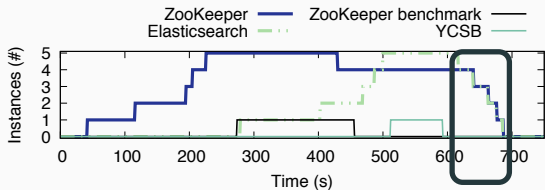
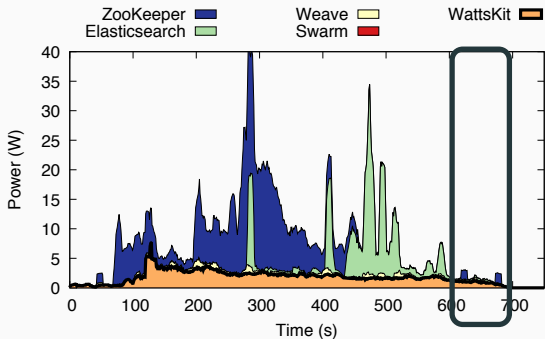
A SERVICE-LEVEL POWER MONITORING



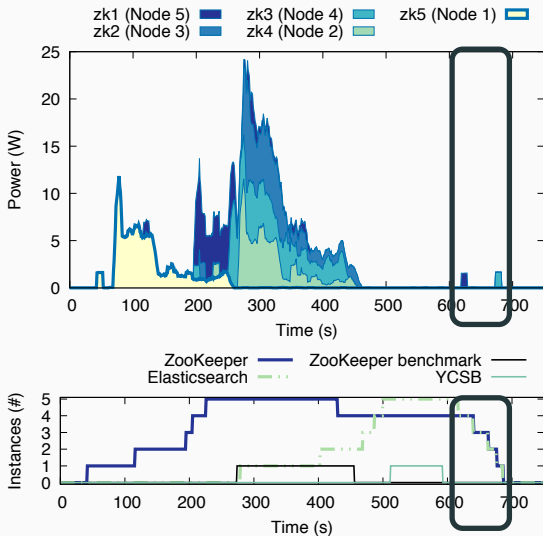
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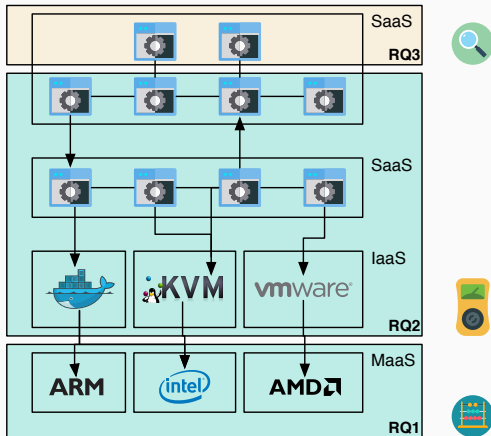
A SERVICE-LEVEL POWER MONITORING



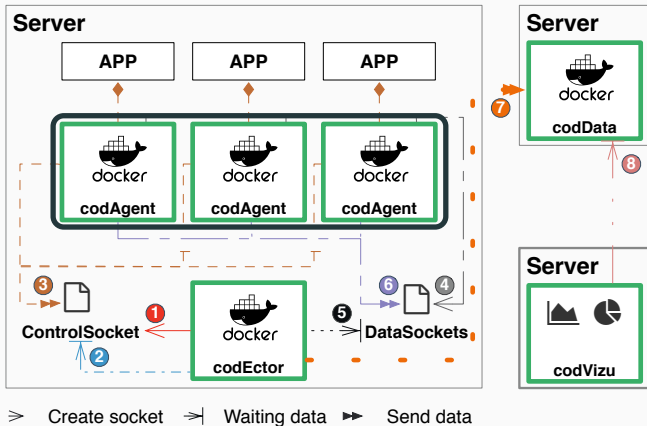
A SERVICE-LEVEL POWER MONITORING



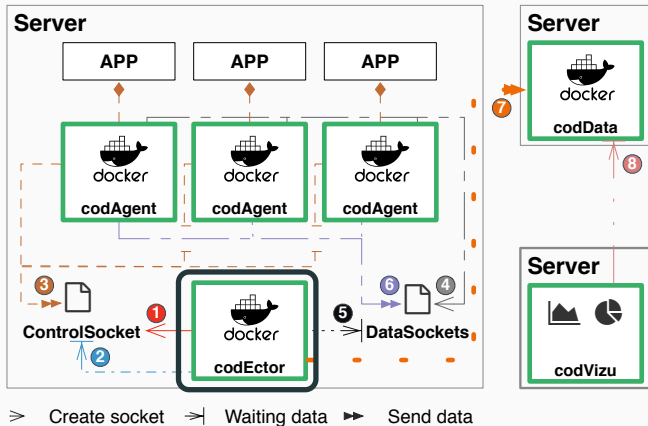
RQ3: Can we analyze the power consumption of the artifacts which compose a software?



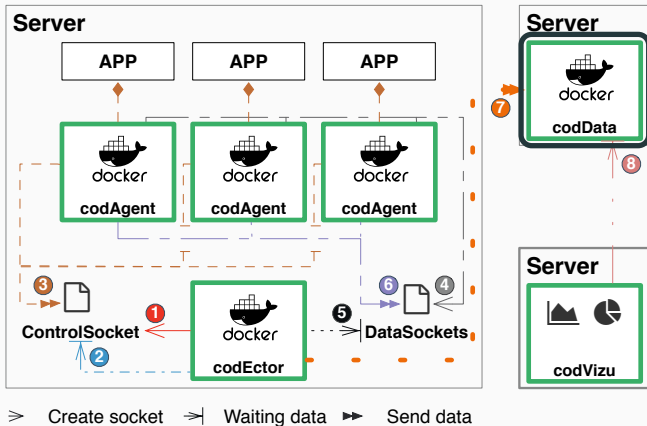
OVERVIEW OF THE CODENERGY APPROACH



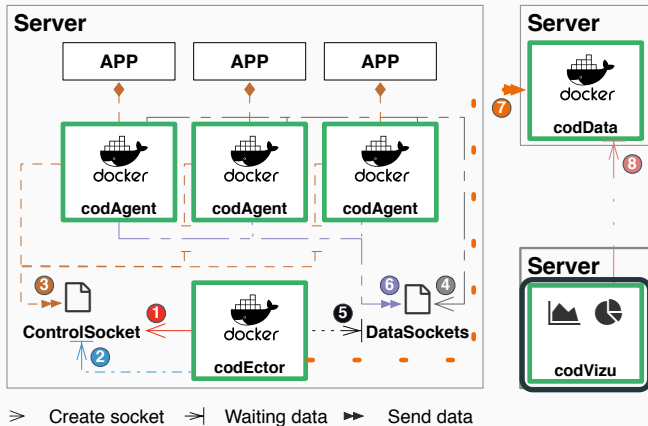
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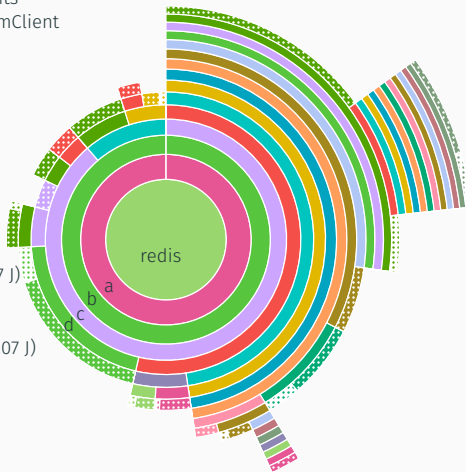
CODVIZU: SUNBURST (1)

a: main
b: aeMain
c: aeProcessEvents
d: readQueryFromClient

 CPU
 DISK

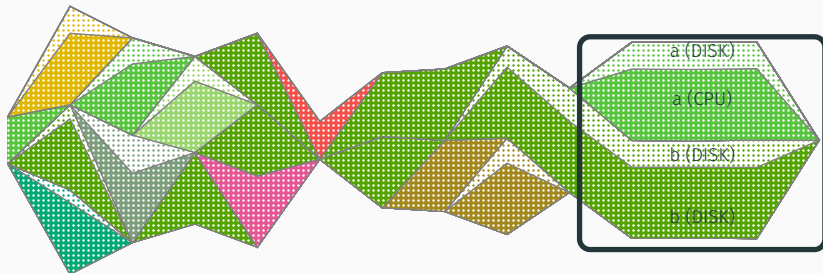
d (DISK)
25.44 J (3.88% of 656.07 J)

d (CPU)
109.41 J (16.68% of 656.07 J)



CODVIZU: STREAMGRAPH (2)

 CPU  DISK



a => readQueryFromClient (CPU): 12.40 W ; readQueryFromClient (DISK): 4.66 W

b => je_huge_ralloc (CPU): 12.34 W ; je_huge_ralloc (DISK): 4.56 W

16:12:18

16:12:20

16:12:22

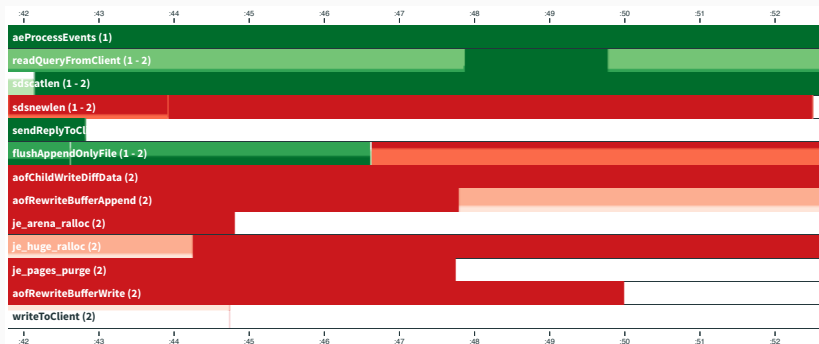
16:12:24

16:12:26

16:12:28

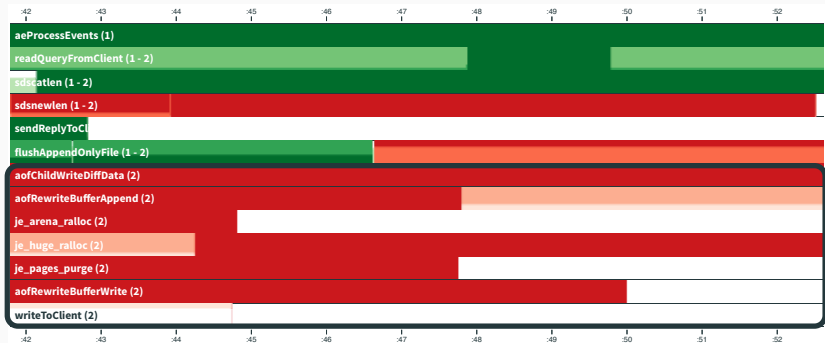
ENERGY DIFFERENCE BETWEEN SOFTWARE SYSTEMS

redis 2 (1) vs redis 3 (2).



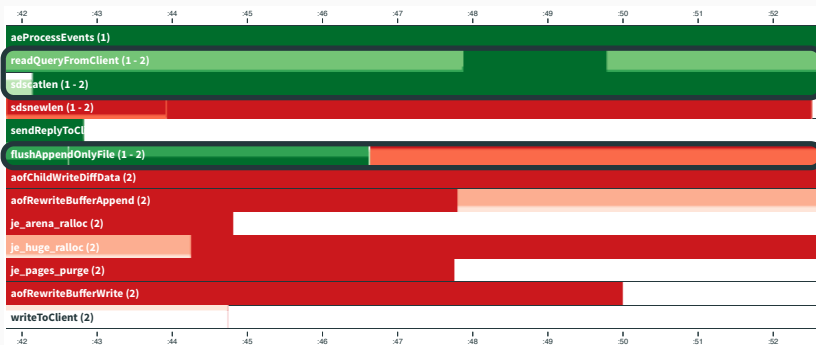
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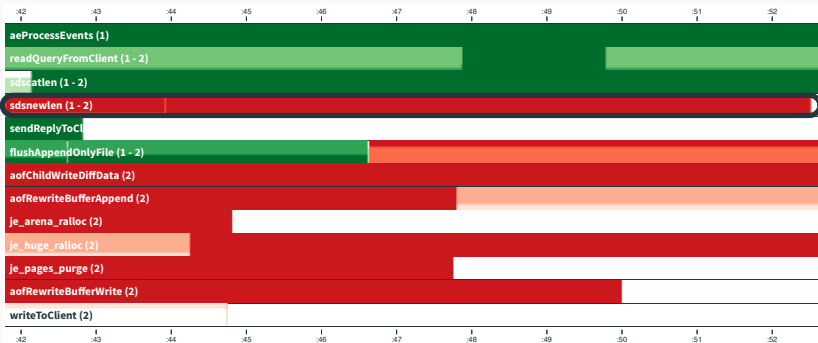
ENERGY DIFFERENCE BETWEEN SOFTWARE SYSTEMS

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CONCLUSION & PERSPECTIVES

Multi-dimensional analysis of software power consumptions on multi-core architectures

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In depth energy monitoring with CODEENERGY

- Define a new scheduler for saving energy in cloud data centers
- Continuous optimization of the power models in a cluster
- Turning-off nodes of a cluster during inactivity periods
- Leveraging source-code energy monitoring
- Extend CODENERGY to other programming languages

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- The power rising of GPU cards
- Proposing a wider energy cartography of a system
- Using genetic programming to improve the energy-efficiency at source-code level
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Thanks for your attention.

Conferences

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Under Evaluation

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